ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a memory cell array, a plurality of latch circuits, first circuit, second circuit and third circuit. The memory cell array has electrically rewritable nonvolatile memory cells arranged therein. The plurality of latch circuits temporarily hold data read out from the memory cell array. The first circuit is configured to generate a first current varying in proportion to "1" or "0" of binary logical data of one end of the plurality of latch circuits. The second circuit is configured to generate a second preset current. The third circuit is configured to compare the first current with the second current. The number of "1" or "0" of binary logical data of one end of the plurality of latch circuits is detected based on the result of comparison between the first current and the second current.